Logarithmic LED panel display has 72-dB range

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Panel-level logarithmic-column displays are usually built around an analog logarithmic converter and a column-display ADC, or the combination of a high-resolution ADC, a processor-controlled logarithmic algorithm, and an LED or LCD column driver.

A simpler, all-digital alternative consists of a serial-output ADC and some timing and display electronics, **Figure 1**.

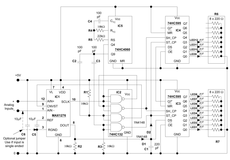

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Figure 1: This stand-alone panel-display circuit drives a 12-LED logarithmic column, whose height changes by one LED for each 6.02 dB change in the input voltage.

A stand-alone circuit, it requires no trimming (as analog versions do), no microcontroller, and no software. The signal to be displayed is applied to a 12-bit ADC (IC1). For the circuit shown, that signal can range from zero (no LED ON) to +2.048 V (all LEDs ON), with the first LED coming ON at +1 mV.

When triggered by a short positive pulse at CNVST, IC1 begins a conversion, clocked by the signal at SCLK. Its output (DOUT) is clocked by the rising edge of SCLK and starts with four leading zeros, followed by the 12-bit conversion result, MSB first. Thus, one conversion result requires 16 clock pulses at SCLK.

The display is a vertical stack of 12 LEDs in which the top LED represents the MSB. During operation, the circuit scans each conversion result as it is generated (MSB first, as described above), notes the first bit with value "1," and then proceeds to illuminate that LED and all those below it. The result is a logarithmic column in which the input-voltage change necessary to move the column one step up or down is double or half the current input value (a 6.02 dB step). The number of steps available equals the ADC resolution (12 bits in this case).

At DOUT, the first output bit with a value of "1" charges C1 (via D1) to the logic-one level. The voltage on C1 connects to the data input (DS) of the first of two cascaded 74HC595 ICs, which together form a 16-bit shift register. The signal that clocks the ADC, slightly delayed, also clocks the shift register, and thereby inserts into the shift register the value presented at its input. At the end of the conversion, all bits following the first one to exhibit a "1" value are also forced to "1" by the voltage stored on C1.

After each conversion is finished, a negative pulse applied to the SC_TP inputs of both the 74HC595 ICs (**Figure 2**) transfers the internal shift-register contents to an internal parallel-output register.

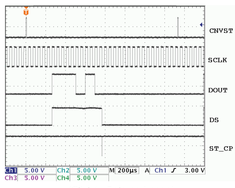

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Figure 2: Timing for the Figure 1 circuit.
CNVST is MAX1276 Conversion trigger signal;
SCLK is MAX1276 Conversion clock, and 74HC595 shift clock;
DOUT is MAX1276 Conversion data out;
DS is 74HC595 shift data input;
ST_CP is 74HC595 Shift register to parallel register transfer clock pulse.

The same pulse discharges the storage capacitor through diode D2, leaving the circuit ready for the next conversion scan. The parallel-register outputs then serve as the column LED drivers. A 74HC4060 IC serves as clock and timing sequence generator, and a 74HC132 provides some necessary glue logic.

Thus, the LED column is a 12-step log indicator with 6-dB step height, forming a total column range of 72 dB. Its accuracy and stability are defined by the specifications for IC1. The sampling rate for the display is about 2.5 kHz, with the component values shown.

About the authors

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